IN THE CLAIMS:

Please cancel claims 14, 17-19 and 21 in their entirety without prejudice nor disclaimer of the subject matter set forth therein

Please amend claim 20 and add new claims 23-29 as follows.

1-3. (Canceled)

4. (Previously Presented) The passive element chip according to Claim 20, wherein the plurality of passive elements includes passive elements of a plurality of specifications.

5. (Original) The passive element chip according to Claim 4, wherein the specifications include a resistance value, a capacitance value, an inductance value, and a quality factor value.

6. (Previously Presented) The passive element chip according to Claim 20, wherein the plurality of passive elements is divided into a plurality of groups having mutually different specifications.

7. (Original) The passive element chip according to Claim 6, wherein the plurality of groups includes a group of high-frequency specifications and a group of low-frequency specifications.

8. (Original) The passive element chip according to Claim 6, wherein the groups include a group composed only of inductors, a group composed only of capacitors, or a group composed only of resistors.

9. (Previously Presented) The passive element chip according to Claim 20, wherein the plurality of passive elements includes only passive elements of high-frequency specifications or only passive elements of low-frequency specifications.

10. (Previously Presented) The passive element chip according to Claim 20, wherein the plurality of passive elements is composed only of inductors or capacitors.

11. (Previously Presented) The passive element chip according to Claim 20, wherein the passive elements are inductors formed of the metal wires spirally disposed.

12. (Previously Presented) The passive element chip according to Claim 20, wherein the passive elements are capacitors in which the metal wires constitute parallel plane electrodes.

13.-19. (Canceled)

20. (Currently Amended) A passive element chip comprising:

a substrate;

an insulating layer having a first surface and a second surface opposite to the first surface, wherein the insulating layer is formed on the substrate, and wherein the second surface of the insulating layer is faced to the substrate; ~~formed on the substrate;~~

an inductor formed in the insulating layer by a first metal wire;

a first electrode formed on the first surface of the insulating layer wherein the first electrode is coupled to the inductor;

a capacitor formed in the insulating layer by a second metal wire, wherein the capacitor is isolated from the inductor;

a second electrode formed on the first surface of the insulating layer, wherein the second electrode is coupled to the capacitor;

a protective film formed on the first surface of the insulating layer, wherein the protective film has a first opening for exposing the first electrode ~~the inductor~~ and a second opening for exposing the second electrode ~~the capacitor~~;

a first wiring pattern formed within the first opening; and

a second wiring pattern formed within the second opening.

21. (Canceled)

22. (Previously Presented) A highly integrated module comprising:

a first substrate;

an insulating film formed on the first substrate;

a passive element chip within the insulating film and being formed on the first substrate, and

a semiconductor chip within the insulating film and being formed on the first substrate;

wherein the passive element chip comprises:

a second substrate different from the first substrate;

an insulating layer formed on the second substrate;

an inductor formed in the insulating layer by a first metal wire;

a capacitor formed in the insulating layer by a second metal wire, with the capacitor being isolated from the inductor; and

a protective film formed on the insulating layer.

23. (New) The passive element chip according to claim 21, further comprising:

a resin layer formed on the protective film, wherein the resin layer has a third opening formed on a first metal post connecting to the first wiring pattern and a fourth opening formed a second metal post connecting to the second metal patter.

24. (New) The passive element chip according to Claim 22, wherein the plurality of passive elements includes passive elements of a plurality of specifications.

25. (New) The passive element chip according to Claim 22, wherein the plurality of passive elements is divided into a plurality of groups having mutually different specifications.

26. (New) The passive element chip according to Claim 22, wherein the plurality of passive elements includes only passive elements of high-frequency specifications or only passive elements of low-frequency specifications.

27. (New) The passive element chip according to Claim 22, wherein the plurality of passive elements is composed only of inductors or capacitors.

28. (New) The passive element chip according to Claim 22, wherein the passive elements are inductors formed of the metal wires spirally disposed.

29. (New) The passive element chip according to Claim 22, wherein the passive elements are capacitors in which the metal wires constitute parallel plane electrodes.